Wireless Components

ASK Single Conversion Receiver

TDA 5200 Version 2.9

Specification January 2007

Revision History		
Current Version: 2.9 as of 10.01.07		
Previous Version: 2.8 as of 01.07.2004		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
3-10, 4-6	3-10, 4-6	Additional info: LO injection mode depending on the RF-range

Edition 01.07

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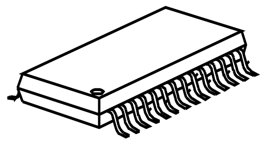
Product Info

General Description

The IC is a very low power consumption single chip ASK Single Conversion Receiver for the frequency bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (I_S = 4.8mA typ. at 868MHz, I_S = 4.6mA typ. at 434MHz)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ)
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity < –107dBm
- Selectable frequency ranges 868-870 MHz and 433-435 MHz
- Limiter with RSSI generation, operating at 10.7MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5200	SP000016381	PG-TSSOP-28
available on tape and reel		

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2 Product Description

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2.1 Overview

The IC is a very low power consumption single chip ASK Single Conversion Receiver for the frequency bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (I_S = 4.8 mA typ. at 868MHz, 4.6mA typ. at 434MHz)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (100nA max.)
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity < –107dBm
- Selectable frequency ranges 868-870 MHz and 433-435 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines

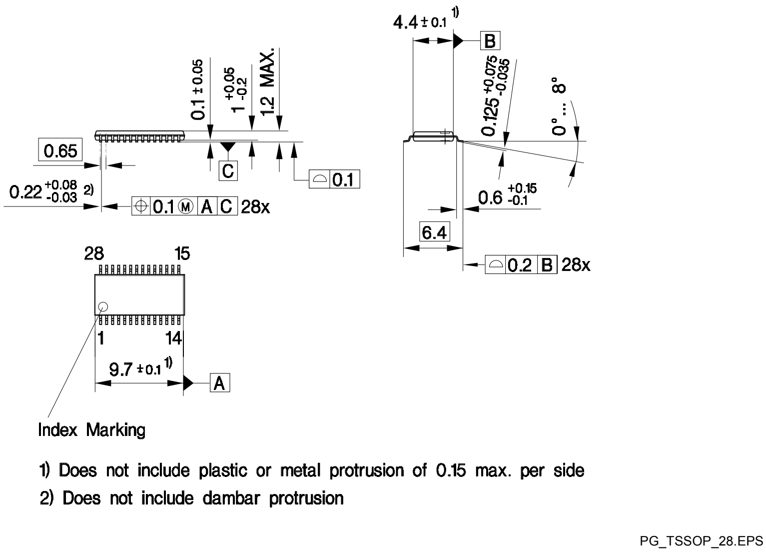

Figure 2-1 PG-TSSOP-28 package outlines

3 Functional Description

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3.1 Pin Configuration

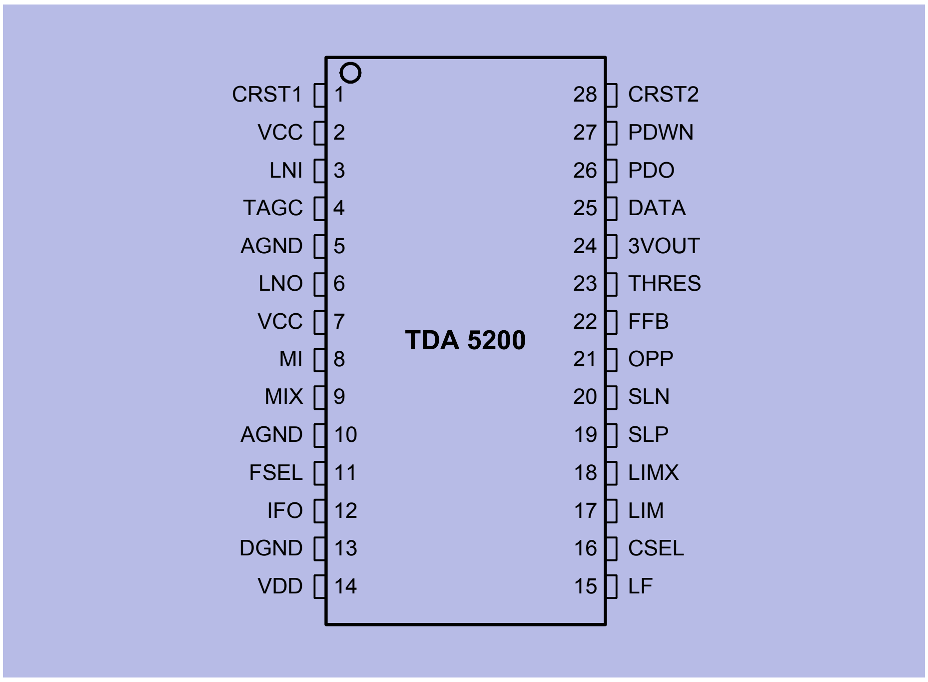
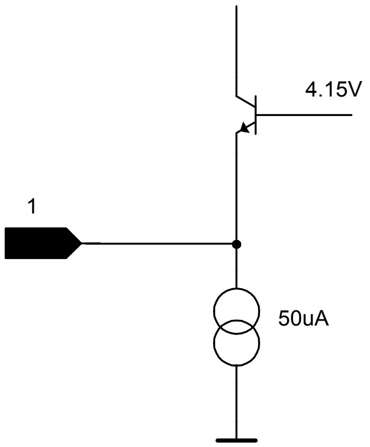
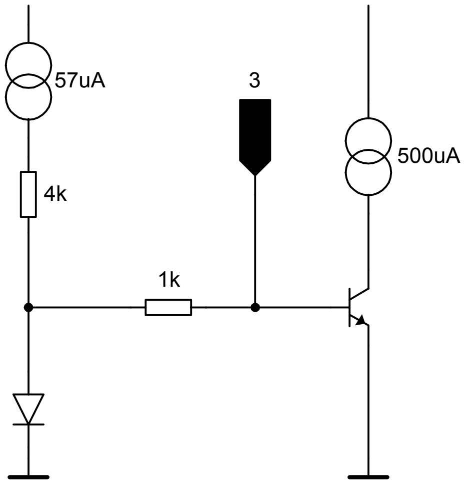
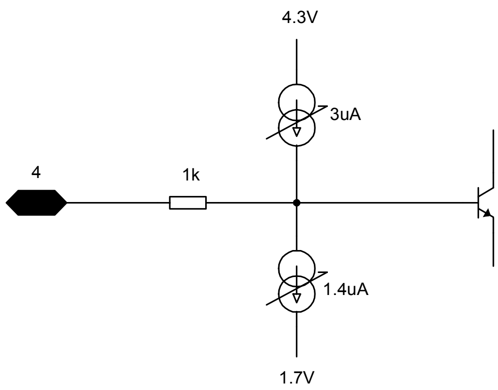
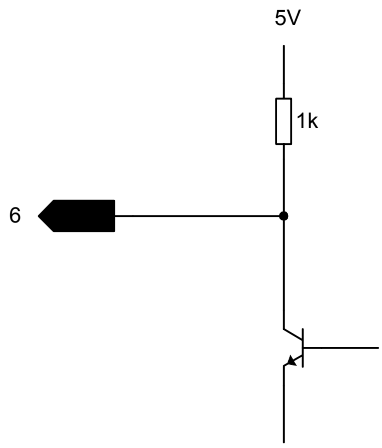
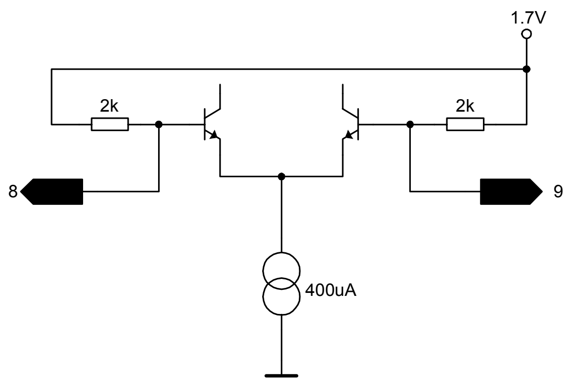


Figure 3-1 IC Pin Configuration

3.2 Pin Definition and Function

Table 3-1 Pin Definition and Function

Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

<table>
<tr><td>4</td><td>TAGC</td><td>
</td><td>AGC Time Constant Control</td></tr>
<tr><td>5</td><td>AGND</td><td></td><td>Analogue Ground Return</td></tr>
<tr><td>6</td><td>LNO</td><td>
</td><td>LNA Output</td></tr>
<tr><td>7</td><td>VCC</td><td></td><td>5V Supply</td></tr>
<tr><td>8
9</td><td>MI
MIX</td><td>
</td><td>Mixer Input
Complementary Mixer Input</td></tr>
<tr><td>10</td><td>AGND</td><td></td><td>Analogue Ground Return</td></tr>
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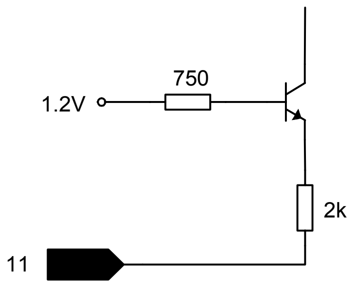
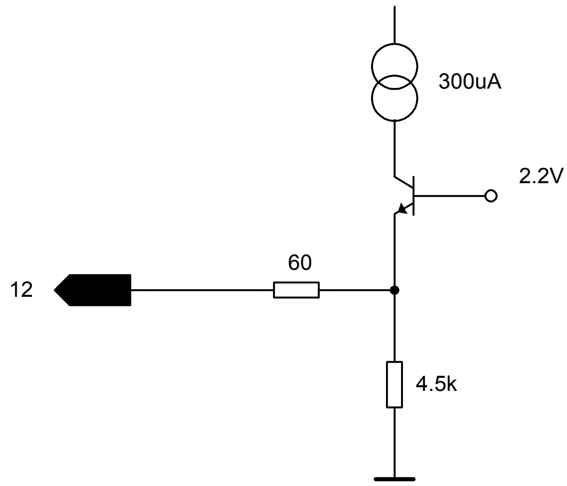
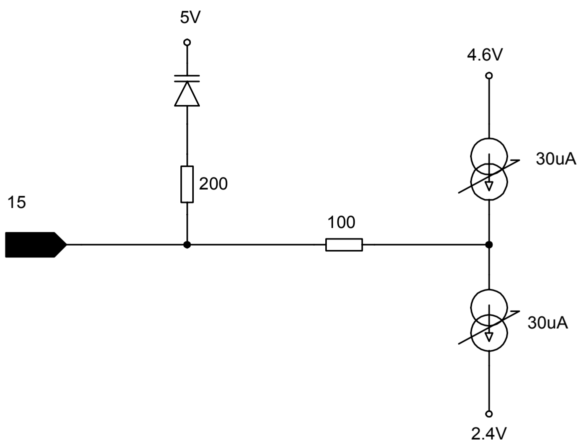
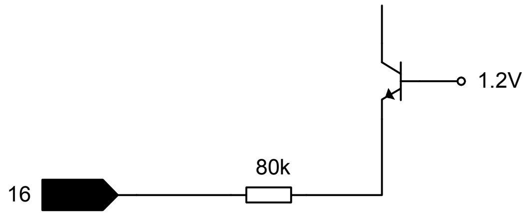
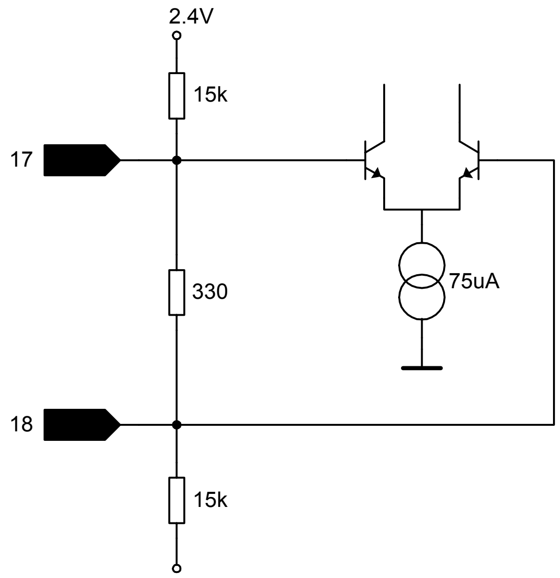
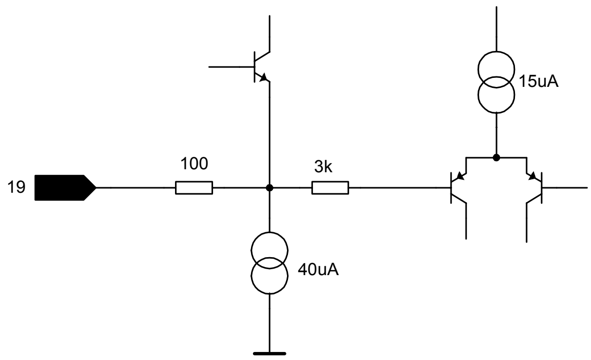
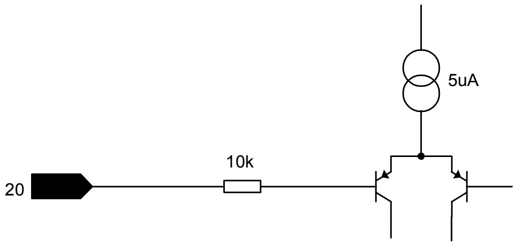
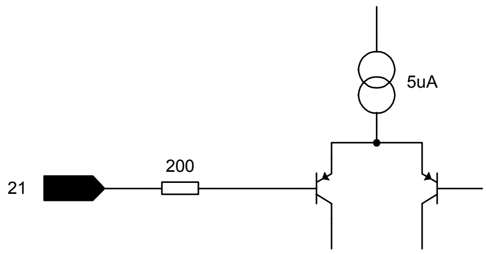
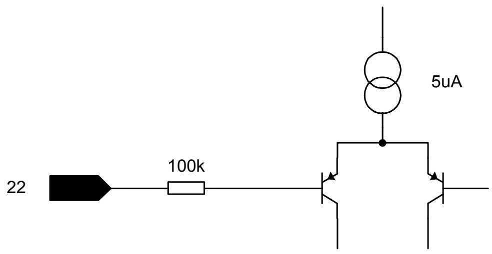
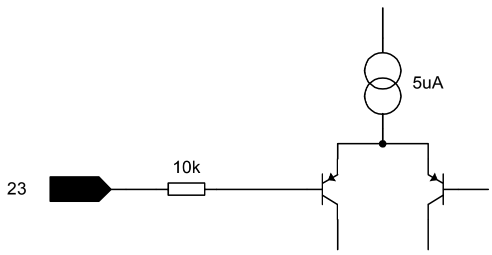
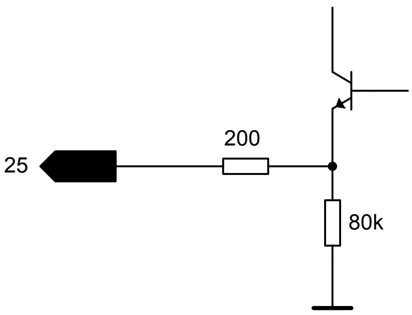
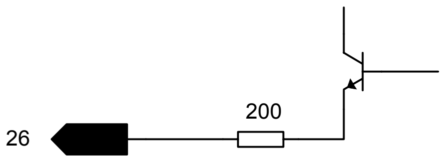
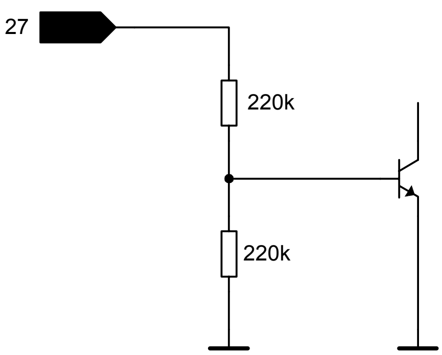
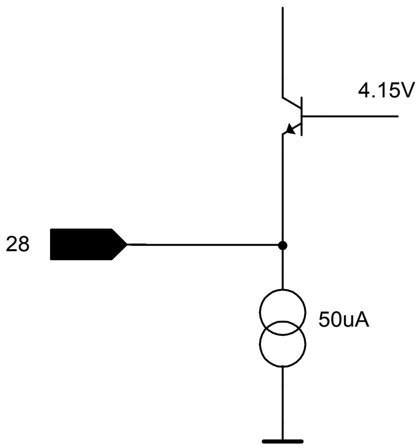
11	FSEL		869/434 MHz Operating Frequency Selector
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	LF		PLL Filter Access Point

16	CSEL		6.xx or 13.xx MHz Quartz Selector
17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input

20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output

<table>
<tr><td>25</td><td>DATA</td><td>
</td><td>Data Output</td></tr>
<tr><td>26</td><td>PDO</td><td>
</td><td>Peak Detector Output</td></tr>
<tr><td>27</td><td>PDWN</td><td>
</td><td>Power Down Input</td></tr>
<tr><td>28</td><td>CRST2</td><td>
</td><td>External Crystal Connector 2</td></tr>
</table>

3.3 Functional Block Diagram

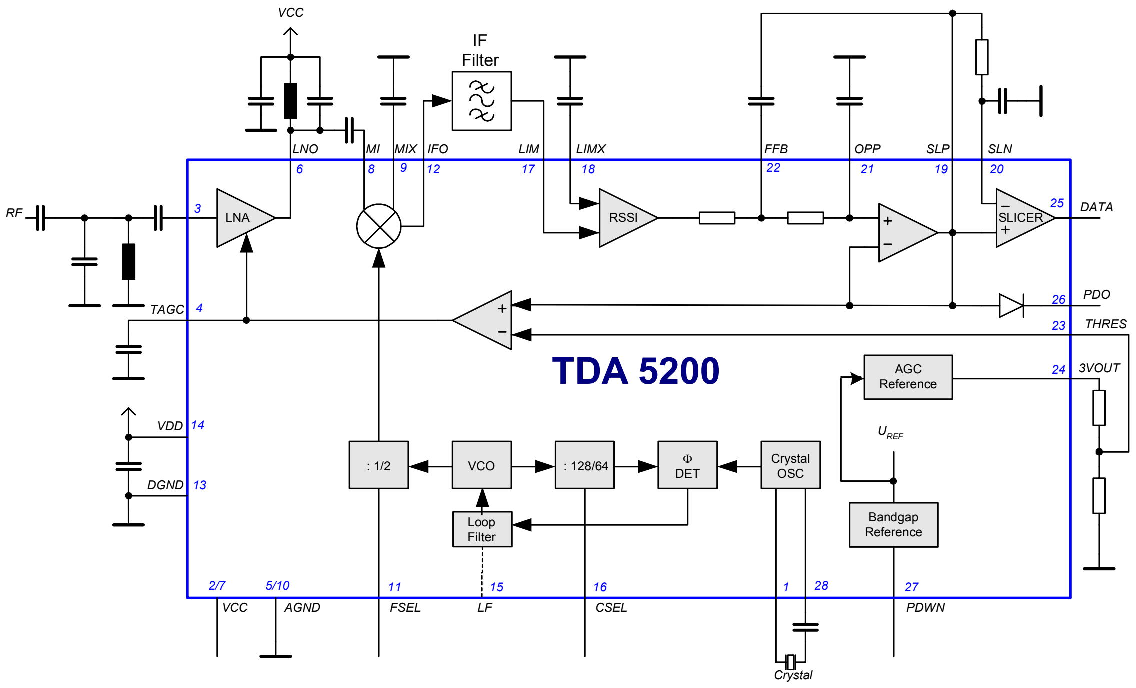


Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3.2dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 433-435MHz/868-870MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB. A low pass filter with a corner frequency of 20MHz is built on chip in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. It's nominal centre frequency is 840MHz. No additional components are necessary.
Local oscillator high side injection has to be used for receive frequencies below approximately 420MHz or 840MHz, low side injection for receive frequencies above approximately 420MHz or 840MHz - see also Section 4.4. Therefore low-side injection of the local oscillator has to be used for operation both in the 868MHz and the 434MHz ISM bands.

The oscillator signal is fed both to the synthesiser divider chain and to the down-converting mixer. In case of operation in the 433 - 435 MHz range, the signal is divided by two before it is fed to the mixer. This is controlled by the selection pin **FSEL** (Pin 11) as described in the following table. The overall division ratio of the divider chain can be selected to be either 128 or 64, depending on the frequency of the reference oscillator quartz (see below). The loop filter is also realised fully on-chip.

Table 3-2 FSEL pin operating states

FSEL	RF Frequency
Open	433 - 435 MHz
Shorted to ground	868 - 870 MHz

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 6 and 13MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-3 CSEL pin operating states

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	13.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is expained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80dB that has a bandpass-characteristic centred around 10.7MHz. It has an input impedance of 330 Ω to allow for easy interfacing to a 10.7MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4-2. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 17dB in case the input signal strength is too strong as described in Section 3.4.1 and Section 4.1.

3.4.6 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.7 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of approximately 120kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on pin 20 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.8 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The output can be used as an indicator for the signal strength and also as a reference for the data slicer. The maximum output current is 500µA.

3.4.9 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA. .

Table 3-4 PDWN pin operating states

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

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4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.

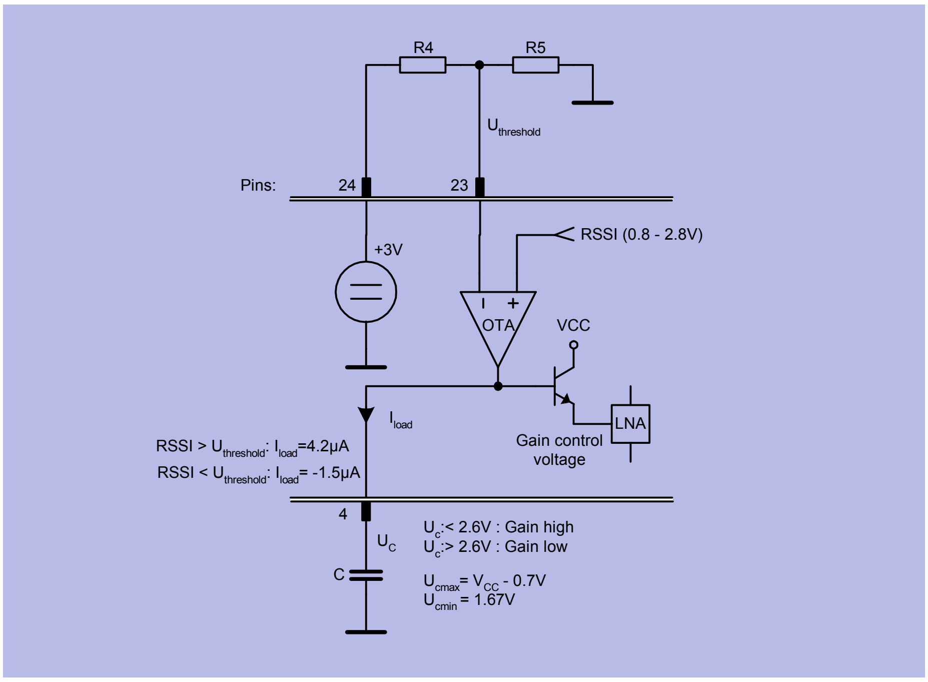
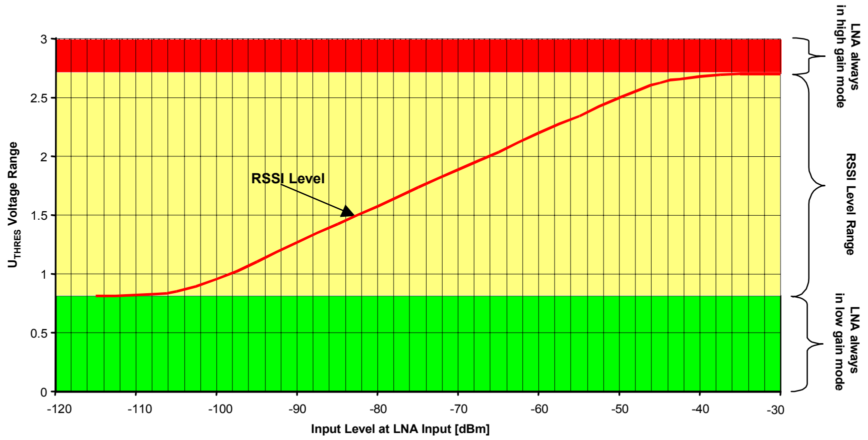


Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.



RSSI-AGC.wmf

Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

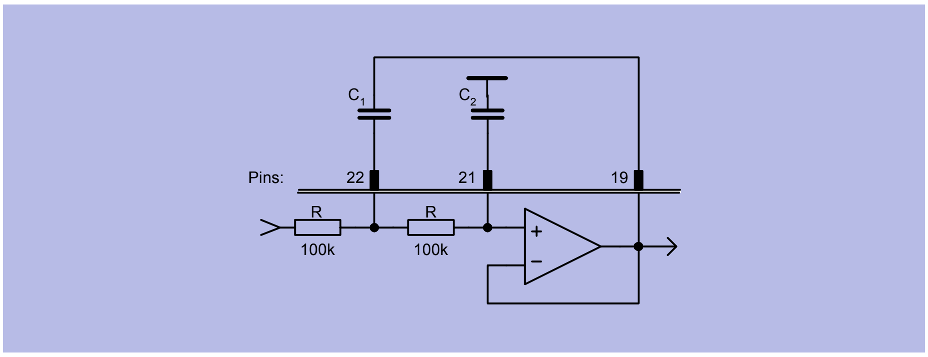
The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the 3VOUT pin is capable of driving up to 50µA, but that the THRES pin input current is only in the region of 40nA. As the current drawn out of the 3VOUT pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. R4 can be chosen as 120kΩ, R5 as 180kΩ to yield an overall 3VOUT output current of 10µA.

Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].



Filter_Design.wmf

Figure 4-3 Data Filter Design

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}}$$

$$C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$

the quality factor of the poles where

in case of a Bessel filter	a = 1.3617, b = 0.618
and thus	Q = 0.577
and in case of a Butterworth filter	a = 1.141, b = 1
and thus	Q = 0.71

Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_1 = 450pF, C_2 = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.

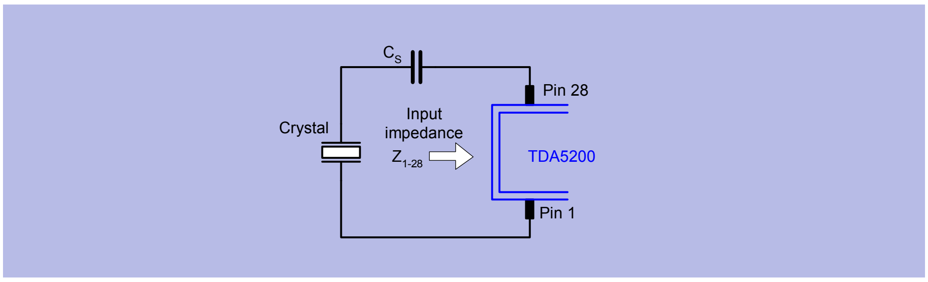


Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L}$$

with C_L the load capacitance (refer to the quartz crystal specification).

Examples:

6.7 MHz:	C_L = 12 pF	X_L=750 Ω	C_S = 8.7 pF
13.401 MHz:	C_L = 12 pF	X_L=1250 Ω	C_S = 5.3 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 20pF and 15pF in the 6.7MHz case and 15pF and 8.2pF in the 13.401MHz case.

But please note that the calculated value of C_S includes the parasitic capacitors also.

4.4 Quartz Frequency Calculation

As described in Section 3.4.3 the operating range of the on-chip VCO is 820 to 860 MHz with a nominal center frequency of approximately 840 MHz. This signal is divided by 2 before applied to the mixer in case of operation at 434 MHz. This local oscillator signal can be used to downconvert the RF signals both with high- or lowside injection at the mixer. The resulting receive frequency ranges then extend between 810 and 870 MHz or between 400 and 440 MHz. Low-side injection of the local oscillator has to be used for receive frequencies between 840 and 870 MHz as well as high-side injection for receive frequencies below 840 MHz. Corresponding to that in the 400 MHz region low-side injection is applicable for receive frequencies above 420 MHz, high-side injection below this frequency. Therefore for operation both in the 868 and the 434 MHz ISM bands low-side injection of the local oscillator has to be used. Then the local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency (434 or 868 MHz). The overall division ratios in the PLL are 64 or 128 in case of operation at 868 MHz or 32 and 64 in case of operation at 434 MHz, depending on the crystal frequency used as shown below.

The quartz frequency is calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{r}$$

with

	f_{RF}	....	receive frequency
	f_{LO}	....	local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)
	f_{QU}	....	quartz oscillator frequency
	r	....	ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table.

Table 4-1 PLL Division Ratio Dependence on States of FSEL and CSEL

FSEL	CSEL	Ratio r = (f_{LO}/f_{QU})
open	open	64
open	GND	32
GND	open	128
GND	GND	64

Subtraction of 10.7 occurs in case the receive frequency is higher than the intended local oscillator frequency, addition in case the receive frequency lies below the local oscillator frequency.

Examples:

$$f_{QU} = (868.4MHz - 10.7MHz)/64 = 13.40156MHz$$

$$f_{QU} = (868.4MHz - 10.7MHz)/128 = 6.7008MHz$$

$$f_{QU} = (434.2MHz - 10.7MHz)/32 = 13.23437MHz$$

4.5 Data Slicer Threshold Generation

The threshold of the data slicer can be generated in two ways, depending on the signal coding scheme used. In case of a signal coding scheme without DC content such as Manchester coding the threshold can be generated using an external R-C integrator as shown in Figure 4-5. The time constant T_A of the R-C integrator has to be significantly larger than the longest period of no signal change T_L within the data sequence. In order to keep distortion low, the minimum value for R is 20kΩ.

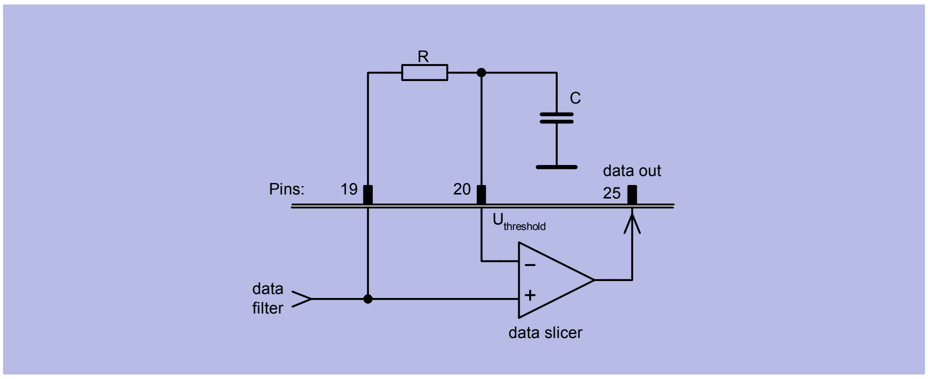


Figure 4-5 Data Slicer Threshold Generation with External R-C Integrator

Another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.

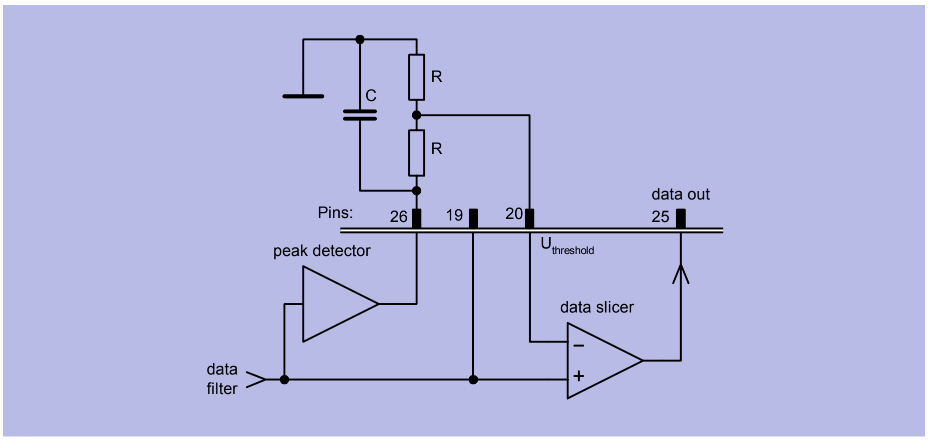


Figure 4-6 Data Slicer Threshold Generation Utilising the Peak Detector

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	V_s	-0.3	5.5	V	
2	Junction Temperature	T_j	-40	+150	°C	
3	Storage Temperature	T_s	-40	+125	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins	V_{ESD}	-1	+1	kV	HBM according to MIL STD 883D, method 3015.7

5.1.2 Operating Range

Within the operating range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed.

Supply voltage: VCC = 4.5V .. 5.5V

Table 5-2 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Test Conditions/ Notes	L	Item
			min	max				
1	Supply Current	$I_{S\ 868}$ $I_{S\ 434}$		5.6 5.4	mA mA	f_{RF} = 868MHz f_{RF} = 434MHz		
2	Receiver Input Level	RF_{in}	-107	-13	dBm	@ source impedance 50Ω, BER 2E-3, average power level, Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
3	LNI Input Frequency	f_{RF}	433/ 868	435/ 870	MHz			
4	MI/X Input Frequency	f_{MI}	433/ 868	435/ 870	MHz			
5	3dB IF Frequency Range	$f_{IF\ -3dB}$	5	23	MHz			
6	Powerdown Mode On	$PWDN_{ON}$	0	0.8	V			
7	Powerdown Mode Off	$PWDN_{OFF}$	2	V_S	V			
8	Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	V_S	V			
9	Gain Control Voltage, LNA low gain state	V_{THRES}	0	0.7V	V			

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in Section 5.2.

5.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. The device performance parameters marked with ■ are not part of production test, but verified by design or measured in an Infineon evaluation board as desdribed in Section 5.2..

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		50	70	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating at 868MHz	$I_{S\ 868}$		4.8	5.2	mA	Pin 11 (FSEL) tied to GND		
3	Supply current, device operating at 434 MHz	$I_{S\ 434}$		4.6	5	mA	Pin 11 (FSEL) open		
LNA									
Signal Input LNI (PIN 3), V_{THRES} > 2.8V, high gain mode									
1	Average Power Level at BER = 2E-3 (Sensitivity)	RF_{in}		-110		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
2	Input impedance, f_{RF}=434 MHz	$S_{11\ LNA}$		0.873 / -34.7 deg				■	
3	Input impedance, f_{RF}=869 MHz	$S_{11\ LNA}$		0.738 / -73.5 deg				■	
4	Input level @ 1dB compression	$P1dB_{LNA}$		-15		dBm		■	
5	Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{LNA}$		-10		dBm	matched input	■	
6	Input 3rd order intercept point f_{RF}=869 MHz	$IIP3_{LNA}$		-14		dBm	matched input	■	
7	LO signal feedthrough at antenna port	LO_{LNI}			-73	dBm		■	
Signal Output LNO (PIN 6), V_{THRES} > 2.8V, high gain mode									
1	Gain f_{RF}=434 MHz	$S_{21\ LNA}$		1.509 / 138.2 deg				■	
2	Gain f_{RF}=869 MHz	$S_{21\ LNA}$		1.419 / 101.7 deg				■	
3	Output impedance, f_{RF}=434 MHz	$S_{22\ LNA}$		0.886 / -12.9 deg				■	

	Parameter	Symbol	Limit Values min	typ	max	Unit	Test Conditions/ Notes	L	Item
Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)									
4	Output impedance, f_{RF}=869 MHz	$S_{22\ LNA}$		0.866 / -24.2 deg				■	
5	Voltage Gain Antenna to Mixer-Out f_{RF}=434 MHz	$G_{AntMixer\ Out}$		42		dB			
6	Voltage Gain Antenna to Mixer-Out f_{RF}=869 MHz	$G_{AntMixer\ Out}$		40		dB			
Signal Input LNI, V_{THRES} = GND, low gain mode									
1	Input impedance, f_{RF}=434 MHz	$S_{11\ LNA}$		0.873 / -34.7 deg				■	
2	Input impedance, f_{RF}=869 MHz	$S_{11\ LNA}$		0.738 / -73.5 deg				■	
3	Input level @ 1dB C. P f_{RF} = 434 MHz	$P1dB_{LNA}$		-18		dBm	matched input	■	
4	Input level @ 1dB C. P f_{RF} = 869 MHz	$P1dB_{LNA}$		-6		dBm	matched input	■	
5	Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{LNA}$		-10		dBm	matched input	■	
6	Input 3rd order intercept point f_{RF}=869 MHz	$IIP3_{LNA}$		-5		dBm	matched input	■	
Signal Output LNO, V_{THRES} = GND, low gain mode									
1	Gain f_{RF}=434 MHz	$S_{21\ LNA}$		0.183 / 140.6 deg				■	
2	Gain f_{RF}=869 MHz	$S_{21\ LNA}$		0.179 / 109.1deg				■	
3	Output impedance, f_{RF}=434 MHz	$S_{22\ LNA}$		0.897 / -13.6 deg				■	
4	Output impedance, f_{RF}=869 MHz	$S_{22\ LNA}$		0.868 / -26.3 deg				■	
5	Voltage Gain Antenna to Mixer-Out f_{RF}=434 MHz	$G_{AntMixer\ Out}$		22		dB			
6	Voltage Gain Antenna to Mixer-Out f_{RF}=869 MHz	$G_{AntMixer\ Out}$		19		dB			
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}		3		V	at 5µA		
2	Current out	I_{3VOUT}			50	µA			
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_S-1V	V	see Section 4.1		

	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
2	LNA low gain mode	V_{THRES}	0			V			
3	LNA high gain mode	V_{THRES}	2.8	3	V_S-1	V	or shorted to Pin 24		
4	Current in	I_{THRES_in}		5		nA		■	
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}		4.2		µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	I_{TAGC_in}		1.5		µA	RSSI < V_{THRES}		
MIXER									
Signal Input MI/MIX (PINS 8/9)									
1	Input impedance, f_{RF}=434 MHz	$S_{11\ MIX}$	0.942 / -14.4 deg					■	
2	Input impedance, f_{RF}=869 MHz	$S_{11\ MIX}$	0.918 / -28.1 deg					■	
3	Input 3rd order intercept point f_{RF}=434 MHz	$IIP3_{MIX}$		-28		dBm		■	
4	Input 3rd order intercept point f_{RF}=869 MHz	$IIP3_{MIX}$		-26		dBm		■	
Signal Output IFO (PIN 12)									
1	Output impedance	Z_{IFO}		330		Ω			
2	Conversion Voltage Gain f_{RF}=434 MHz	G_{MIX}		+19		dB			
3	Conversion Voltage Gain f_{RF}=869 MHz	G_{MIX}		+18		dB			
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	Input Impedance	Z_{LIM}	264	330	396	Ω		■	
2	RSSI dynamic range	DR_{RSSI}	60		80	dB			
3	RSSI linearity	LIN_{RSSI}		±1		dB		■	
4	Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz		■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values min	typ	max	Unit	Test Conditions/ Notes	L	Item
Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)									
DATA FILTER									
1	Useable bandwidth	BW_{BB} FILT			100	kHz		■	
2	RSSI Level at Data Filter Output SLP	$RSSI_{low}$		1.1		V	LNA in high gain RF_{IN}=-103dBm 868MHz		
3	RSSI Level at Data Filter Output SLP	$RSSI_{high}$		2.65		V	LNA in high gain. RF_{IN}=-30dBm 868MHz		
SLICER									
Signal Output DATA (PIN 25)									
1	Useable bandwith	BW_{BB} SLIC			100	kHz		■	
2	Capacitive loading of output	C_{max} SLIC			20	pF			
3	LOW output voltage	V_{SLIC_L}		0		V			
4	HIGH output voltage	V_{SLIC_H}	V_S-1.3	V_S-1	V_S-0.7	V	Output current =200µA		
5	Output current	I_{SLIC_out}			200	µA			
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	LOW output voltage	V_{SLIC_L}		0		V			
2	HIGH output voltage	V_{SLIC_H}			V_S-1	V			
3	Load current	I_{load}	-500			µA	Static load current must not exceed -500µA		
4	Leakage current	$I_{leakage}$		700		nA			
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRISTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	6		14	MHz	fundamental mode, series resonance		
2	Input Impedance @ ~6MHz	Z_{1-28}		-900 +j750		Ω		■	
3	Input Impedance @ ~13MHz	Z_{1-28}		-450 +j1250		Ω		■	
4	Serial Capacity @ ~6MHz	$C_{S\ 6}$=C1		8.7		pF			
5	Serial Capacity @ ~13MHz	C_{S13}=C1		5.3		pF			

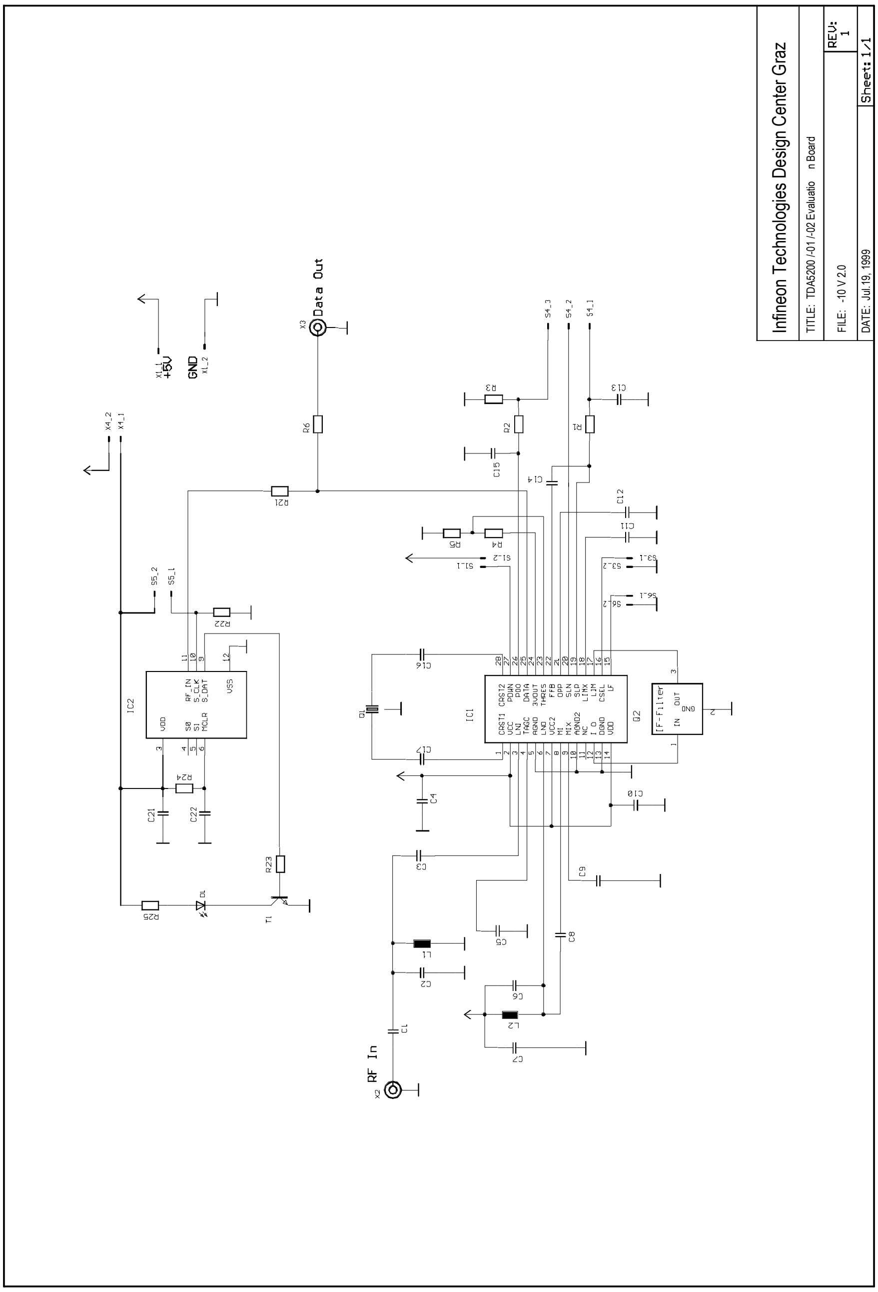
	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
PLL									
Signal LF (PIN 15)									
1	Tuning voltage relative to V_s	V_{TUNE}	0.4	1.6	2.4	V			
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	2.8		V_S	V			
2	Powerdown Mode Off	$PWDN_{Off}$	0		0.8	V			
3	Input bias current PDWN	I_{PDWN}		19		µA			
4	Start-up Time until valid IF signal is detected	T_{SU}		<1		ms	depends on the used crystal		
VCO MULTIPLEXER									
Signal FSEL (PIN 11)									
1	f_{RF} range 434 MHz	V_{FSEL}	1.4		4	V	or open		
2	f_{RF} range 869 MHz	V_{FSEL}	0		0.2	V			
3	Input bias current FSEL	I_{FSEL}		200		µA	FSEL tied to GND		
PLL DIVIDER									
Signal CSEL (PIN 16)									
1	f_{CRSTL} range 6.xxMHz	V_{CSEL}	1.4		4	V	or open		
2	f_{CRSTL} range 13.xxMHz	V_{CSEL}	0		0.2	V			
3	Input bias current CSEL	I_{CSEL}		5		µA	CSEL tied to GND		

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in Section 5.2.

5.2 Test Circuit

The device performance parameters marked with ■ in Section 5.1.3 were either verified by design or measured on an Infineon evaluation board. This evaluation board can be obtained together with evaluation boards of the accompanying transmitter device TDA5100 in an evaluation kit that may be ordered on the INFINEON RKE Webpage www.infineon.com/rke



Test_circuit.wmf

Figure 5-1 Schematic of the Evaluation Board

5.3 Test Board Layouts

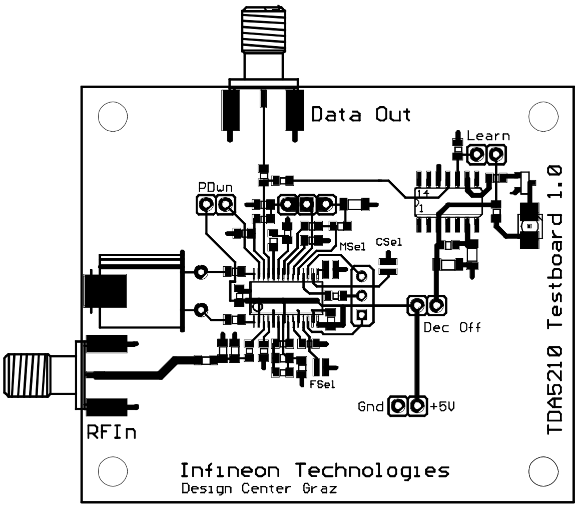


Figure 5-2 Top Side of the Evaluation Board

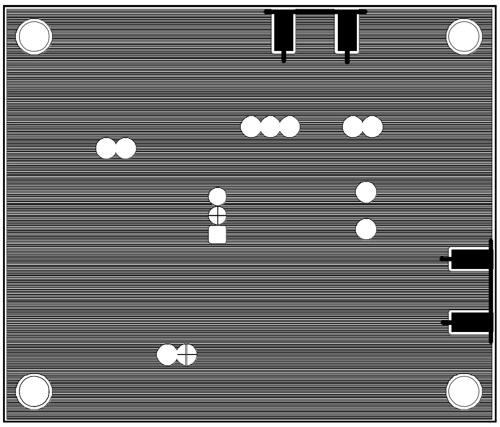


Figure 5-3 Bottom Side of the Evaluation Board

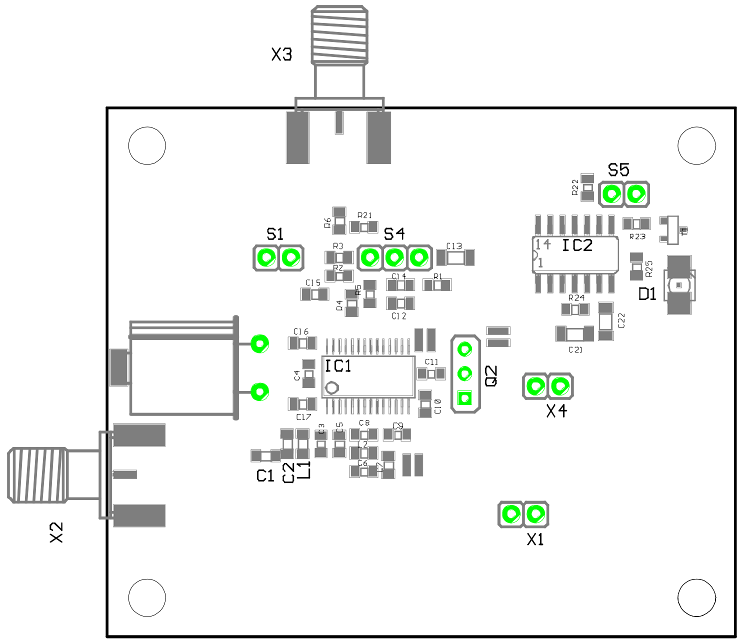


Figure 5-4 Component Placement on the Evaluation Board

5.4 Bill of Materials

The following components are necessary for evaluation of the TDA5200 without use of a Microchip HCS515 decoder.

Table 5-4 Bill of Materials

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R3	820kΩ	0805, ± 5%
R4	120kΩ	0805, ± 5%
R5	180kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	434 MHz: 15nH 869 MHz: 3.3nH	Toko, PTL2012-F15N0G Toko, PTL2012-F3N3C
L2	434 MHz: 8.2pF 869 MHz: 3.9nH	0805, COG, ± 0.1pF Toko, PTL2012-F3N9C
C1	1pF	0805, COG, ± 0.1pF
C2	434 MHz: 4.7pF 869 MHz: 3.9pF	0805, COG, ± 0.1pF 0805, COG, ± 0.1pF
C3	434 MHz: 6.8pF 869 MHz: 5.6pF	0805, COG, ± 0.1pF 0805, COG, ± 0.1pF
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	434 MHz: 10nH 869 MHz: 3.9pF	Toko, PTL2012-F10N0G 0805, COG, ± 0.1pF
C7	100pF	0805, COG, ± 5%
C8	434 MHz: 33pF 869 MHz: 22pF	0805, COG, ± 5% 0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	220pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	470pF	0805, COG, ± 5%
C15	47nF	0805, X7R, ± 5%
C16	15pF	0805, COG, ± 1%
C17	8.2pF	0805, COG, ± 1%
Q2	(f_{RF} – 10.7MHz)/32 or (f_{RF} – 10.7MHz)/64	HC49/U, fundamental mode, CL = 12pF, e.g. 434.2MHz: Jauch Q 13,23437-S11-1323-12-10/20 e.g. 868.4MHz: Jauch Q 13,40155-S11-1323-12-10/20

Table 5-4 Bill of materials (continued)		
Ref	**Value**	**Specification**
F1	SFE10.7MA5-A or SKM107M1-A20-10	Murata Toko
X2, X3	142-0701-801	Johnson
X1, X4, S1, S5		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA 5200	Infineon

Please note that in case of operation at 434 MHz a capacitor has to be soldered in place of L2 and an inductor in place of C6.

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA52o0 in conjunction with a Microchip HCS515 decoder.

Table 5-5 Bill of Materials Addendum		
Ref	**Value**	**Specification**
R21	22kΩ	0805, ± 5%
R22	100kΩ	0805, ± 5%
R23	22kΩ	0805, ± 5%
R24	820kΩ	0805, ± 5%
R25	560kΩ	0805, ± 5%
C21	100nF	1206, X7R, ± 10%
C22	100nF	1206, X7R, ± 10%
IC2	HCS515	Microchip
T1	BC 847B	Infineon
D1	LS T670-JL	Infineon

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